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REMARKS

Claims 8-19 are pending and have been rejected. Claim 8 has been amended to clarify the antecedent basis for "first source, drain and channel regions" and "second source, drain and channel regions" in claims 10 to 17. No new issue requiring further search or consideration is necessitated by this amendment as claim 8 already specified that source, drain and channel regions were made in each of the ***first*** and ***second*** transistor regions, so that it already was clear that the first source, drain and channel were those in the first transistor region and the second source, drain and channel were those in the second transistor region. Entry of the amendments to claim 8 after final rejection therefore are believed proper. Additionally, the dependency of claim 13 has been changed, and claims 18 and 19 have been canceled. Claims 8-17 remain in the case.

Claims 8-11, 18 and 19 are rejected under Section 103(a) based on Gardner (U.S. Patent No. 5,885,874) in view of Osanai (U.S. Patent No. 6,653,694). The examiner alleges that Gardner shows ***most*** aspects of the instant invention, including:

forming a well region in a semiconductor substrate 102 of a first-conductivity-type (N) with a first region 106 and a second region 108

forming a gate insulating film 110, gate electrodes 126, 128 and source/drain regions 150, 152, 154, 156,

forming field oxide regions 104 separating the first and second regions.

implanting ions 116, 122 of a first-conductivity-type into the first and second regions

implanting ions of a second-conductivity-type 148 to permit current flow 140, and

stating that the invention is used in microprocessors which can contain masked ROMs and that the dopants used can be either N or P.

Gardner was discussed in applicant's last response. It discloses a method of providing a semiconductor substrate with first and second device regions, forming a gate material over the first and second device regions, and then implanting a dopant into the gate material such that a peak concentration of the dopant has a first depth in the gate material over the first device region and a second depth in the gate material over the second device region, the first depth being substantially greater than the second depth. After implanting the dopant into the gate material, the gate material is etched to form a first gate over the first device region and a second gate over the second device region. Source and drains are formed in the first and second device regions, and then the dopant in the gate material is transferred into a first channel region in the first device region without transferring essentially any of the dopant into a second channel region in the second device region. This provides depletion-mode doping in the first channel region while retaining enhancement-mode doping in the second channel region.

According to the present invention, on the other hand, a first transistor of a MIS depletion type and a second transistor forming part of a masked ROM are formed on a single semiconductor substrate by forming a well region of a first-conductivity-type in a first region where the first transistor is to be formed and a second region where the second transistor is to be formed, implanting impurity ions of a first-conductivity-type in the regions where the first and second transistors are to be formed to form a channel region, implanting impurity ions of a second-conductivity-type in the channel regions of the first and second transistors to permit current to flow when a gate-source voltage of the first transistor is zero and to change the second transistor into resistance, said implanting of impurity ion of said second conductivity type in both of said channel regions being carried out in the same ion implantation step; and thereafter forming a gate insulating film, a gate electrode, and source and drain regions of a

second-conductivity-type in each of the first and second transistors. This is clearly distinct from the process of Gardner, in which a dopant is implanted into a gate material and then is transferred into a first channel region in a first device region without transferring essentially any of the dopant into a second channel region in a second device region. Claim 8 has been amended to emphasize that the gate in the process according to the present invention is formed after the formation of the channel regions, that the implanting of impurity ions of the second-conductivity-type is into the channel regions of the first and second to permit current to flow when a gate-source voltage of the first transistor is zero and to change the second transistor into resistance, and that said implanting of impurity ion of said second conductivity type in both of said channel regions being carried out in the same ion implantation step. This is not disclosed or suggested by the process of Gardner.

The examiner admits that Gardner does not show the implanting of second-conductivity type ions into the channel regions in the same ion implantation. He alleges, however, that Osanai would have suggested this feature, citing Column 7, line 38 to Column 8, line 12 and Figure 10.

The cited portion of Osanai discloses that after P-wells 102 and 103 are formed in the N-type semiconductor substrate 101, a field insulting film 105 is formed to isolate the E-type and D-type NMOS structures. Then an impurity is doped into the region that will be the channel region in each structure by ion injection. Osanai discloses that the impurity doping is for threshold control, and discloses that "it is possible to simultaneously form both the NMOSs by the same process in accordance with the threshold voltage." The cited impurity doping in Osanai is done to form the channel region, and ***is not*** the doping of a second conductivity type into already-formed channel regions.

The examiner's attention is directed to paragraphs 0044 to 0047 of applicant's specification and Figure 1. Figure 1 shows P type well region 2 formed on the principal side of the P type semiconductor substrate 1. Field oxide film 3 for separating elements is formed on

the entire surface of the well region 2 and separates the depletion MOS transistor 101 and the masked ROM transistor 102 from each other. Then channel region 13 is formed by implanting ions to form a P^- channel region. Channel region 23, on the other hand, initially is a P^+ channel region. Both of these regions are implanted at the same time with ions of a second conductivity type. This second implantation step converts P^+ channel region 23 into resistance at the same time that P^- channel region 13 is changed to an N^- depletion region.

Osanai discloses that channel regions for both the E-type and D-type NMOS can be formed simultaneously, *i.e.*, the same ions/dosage can be used for implanting channels into the P wells for both devices. Then the two devices are separately masked in Figures 11 and 12, and different ions/dosages are used to make the two devices. In Figure 11, phosphorus or arsenic is implanted in a deposited polycrystalline silicon layer to form an N^+ gate electrode for a D-type NMOS. In Figure 12, BF_2 is implanted in the polycrystalline silicon layer to form a P^+ gate electrode for an E-type NMOS.

Thus, Osanai creates channel regions for two devices with a single implantation step and then subsequently forms gate electrodes of differing conductivity types for the two devices in separate implantation steps. This is in clear contrast to the present invention, which starts with differing channel regions for two devices, then uses a single implantation step. As described in paragraph 0043, according to the present invention, the semiconductor integrated circuit device can be formed by implanting impurity ions to change the transistor forming the masked ROM into resistance while implanting ions for changing the enhancement type transistor into the depletion type transistor, so that at least a depletion type MIS transistor and a transistor forming a masked ROM can be integrated into a single semiconductor substrate. Further, a submicron CMOS can be integrated with the depletion type MIS transistor and the transistor forming the masked ROM can be integrated into a single semiconductor substrate.

The implantation of impurity ions for changing the enhancement type transistor into the depletion type transistor and the implantation of impurity ions for changing the transistor

constituting the masked ROM into resistance can be carried out by the same ion implantation process. This implantation step permits current to flow in one of the devices when gate-source voltage of zero and converts the other device into resistance. That is, applicant's channel region 23 is formed by changing a P^+ channel region formed in the channel region 23 into resistance by implantation of ions at the same time as implantation of ions for regulating a threshold voltage of another transistor. There is no suggestion in the combination of Gardner and Osanai of this method.

Claims 12-15 are rejected under Section 103(a) based on Gardner (U.S. Patent No. 5,885,874) in view of Osanai (U.S. Patent No. 6,653,694) in further view of Oda *et al.* (U.S. Patent No. 6,469,347). Gardner and Osanai are discussed above. Oda *et al.* is cited as disclosing punch-through stopper regions and NMOS in P wells. Oda *et al.* does not overcome the failure of Gardner and Osanai to disclose the features of the invention that are recited in independent claim 8, and therefore no *prima facie* case of obviousness exists with respect to claims 12 to 15.

If there are any problems with this response, Applicant's attorney would appreciate a telephone call. In view of the foregoing, it is believed none of the references, taken singly or in combination, disclose the claimed invention. Accordingly, this application is believed to be in condition for allowance, the notice of which is respectfully requested

Respectfully submitted,

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Date

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